Call for Papers

IEEE Asian Solid-State Circuits Conference
A-SSCC 2020

Location: Grand Prince Hotel Hiroshima, Hiroshima, Japan

Date: November 9 – 11, 2020

Sponsored by IEEE SSCS, IEEE Region-10 SSCS Chapters

http://www.asscc.org

http://sscs.ieee.org

Conference Theme: Intelligent Chips for AIoT Era

The development of artificial intelligence of things (AIoT), which combines artificial intelligence (AI) and internet of things (IoT), enables new digital services to elevate customer experiences and accelerate business performance. With the advancement of solid-state circuits, intelligent chips can provide powerful computation capabilities to analyze the information through patterns, visions, and sounds. By moving part of the computing to the edge, the devices perform less time for communication, low latency, and reliable operation in offline periods. The innovations of intelligent chips will lead us to the era of AIoT.

The IEEE A-SSCC 2020 (Asian Solid-State Circuits Conference) is an international forum for presenting the most updated and advanced chips and circuit designs in solid-state and semiconductor fields. The conference is supported by the IEEE Solid-State Circuits Society and will be held in Asia. Further details on the conference and paper submission guidelines and templates will be available at the A-SSCC official website http://www.asscc.org/ (or http://www.a-sscc2020.org/) around the beginning of April 2020.

Paper Submission

Prospective authors are invited to submit four-page or two-page manuscripts, including figures, tables and references, to the official A-SSCC 2020 website. The two-page submission could include two-page supplements with figures and figure captions. Supplementary figures should not be referred to in the text of the paper. For further details, see the A-SSCC Website. Papers are solicited in the following categories:

Regular Session

1. **Analog Circuits & Systems:** Amplifiers, comparators, switched capacitor circuits, continuous-time & discrete-time filters, voltage/current references; DC-DC converters, power-control circuits; IF/baseband analog circuits, AGC/VGA; non-linear analog circuits.
2. **Data Converters:** Nyquist-rate and oversampling A/D, D/A converters, time-to-digital converters, and capacitance-to-digital converters; sub-circuits for data converters including sample-and-hold circuits, calibration circuits, etc.
3. **Digital Circuits & Systems:** Design, fabrication, and test of digital VLSI systems; high-speed low-power digital circuits, power-reduction and management methods for digital VLSI, ultra-low-voltage and sub-threshold logic design; leakage reduction techniques; clock distribution, I/O circuits, reconfigurable logic-array circuits; supply/substrate noise measurement and cancellation for digital VLSI, variation and fault-tolerant circuits.
4. **SoC & Signal Processing Systems:** System-on-chip(including 3D integration), microprocessors, network processors, baseband communication processing system & architectures, system-level power management; multimedia and recognition processing systems; cryptographic, security, machine learning, deep-learning, and neuromorphic circuits and systems; bio-medical/neural-network processors and sensor network systems.
5. **RF:** Receivers/transmitters/transceivers for wireless systems; narrowband RF, ultra-wideband and millimeter-wave circuits; circuits and building-blocks including RF front-end, LNA, mixer, power amplifiers, VCOs, frequency synthesizers, RF filters, RF switches, power detectors, active antennas.
6. **Wireline:** Receivers/transmitters/transceivers for wireline systems; optical/electrical data links and backplane transceivers; power-line communication; clock generation circuits, PLL, DLL, spread-spectrum clock generation; building blocks for high-speed wireline communication.
7. **Emerging Technologies and Applications:** Advanced system designs and circuit solutions for technologies and applications including state-of-the-art devices and packaging technologies; flexible and printable electronics; silicon photonics; smart sensors and transducers; MEMS for analog, RF, and sensor applications; image sensors and displays; energy harvesting systems; transceiver systems; medical/bio-electronics/bio-inspired chip design, artificial intelligent system, and cryogenic circuits and systems.
8. **Memory:** Volatile and Non-volatile memory; new memory designs for 3D/2D architectures, emerging devices such as resistive-/phase change-/magnetic-/ferro-electric- memory devices; data storage and multi-bit-cell memory design; cache-memory system, multi-port memory, memory subsystem, processing in memory, and CAM design; yield-enhancing and ECC techniques; memory testing and built-in self-test.
9. **FPGA:** Novel algorithm and/or architecture for integrated circuits validated by FPGA implementation. The authors of accepted papers are required to participate in demo sessions.

Special Session

1. **Industry Program:** This special category accepts only papers based on state-of-the-art industrial products. Strong emphasis on systems realized by silicon chips is encouraged. The papers should cover architecture, circuits, process technology, packaging and testing, including characterization results, die and system photos, as well as product demos.
2. **Student Design Contest:** A student design contest is held among the accepted papers with system prototypes or measurement results of which operations can be demonstrated on-site. Refer to the web for further information.

Extended versions of selected papers from the Conference (including the FPGA track with the fabricated silicon measurement results) will be published in a Special Issue of the IEEE Journal of Solid-State Circuits. Upon acceptance by the A-SSCC, high-quality papers will be solicited for possible cross-publication in the IEEE Solid-State Circuits Letters (SSCL). Such papers will undergo the SSCL standard review process, and some revisions may be requested by the reviewers. Important Notes:

1. The papers accepted and published by the SSCL will be limited to four pages and will be cross-listed by A-SSCC. In other words, only one version of the paper will be published: if a paper accepted by the A-SSCC is also accepted by the SSCL, then only the latter version will be published; conversely, if a paper is accepted by the A-SSCC but not by the SSCL, then only the A-SSCC version will be published on the Proceedings of ASSCC (not on the SSCL).
2. Cross-publication with the SSCL does not preclude publishing an extended paper in the IEEE Journal of Solid-State Circuits.

Prospective authors should note that presentation slides in A-SSCC will be shared by the attendees.

Important dates

Paper submission	**June 1, 2020, 20:00 (GMT)**	**Acceptance notification**	**August 3, 2020**
Final paper submission	**September 6, 2020**		

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